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RENEASAS

# QP<sup>™</sup> Development Kit (QDK) Renesas RX with IAR

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[info@quantum-leaps.com](mailto:info@quantum-leaps.com)  
[www.state-machine.com](http://www.state-machine.com)

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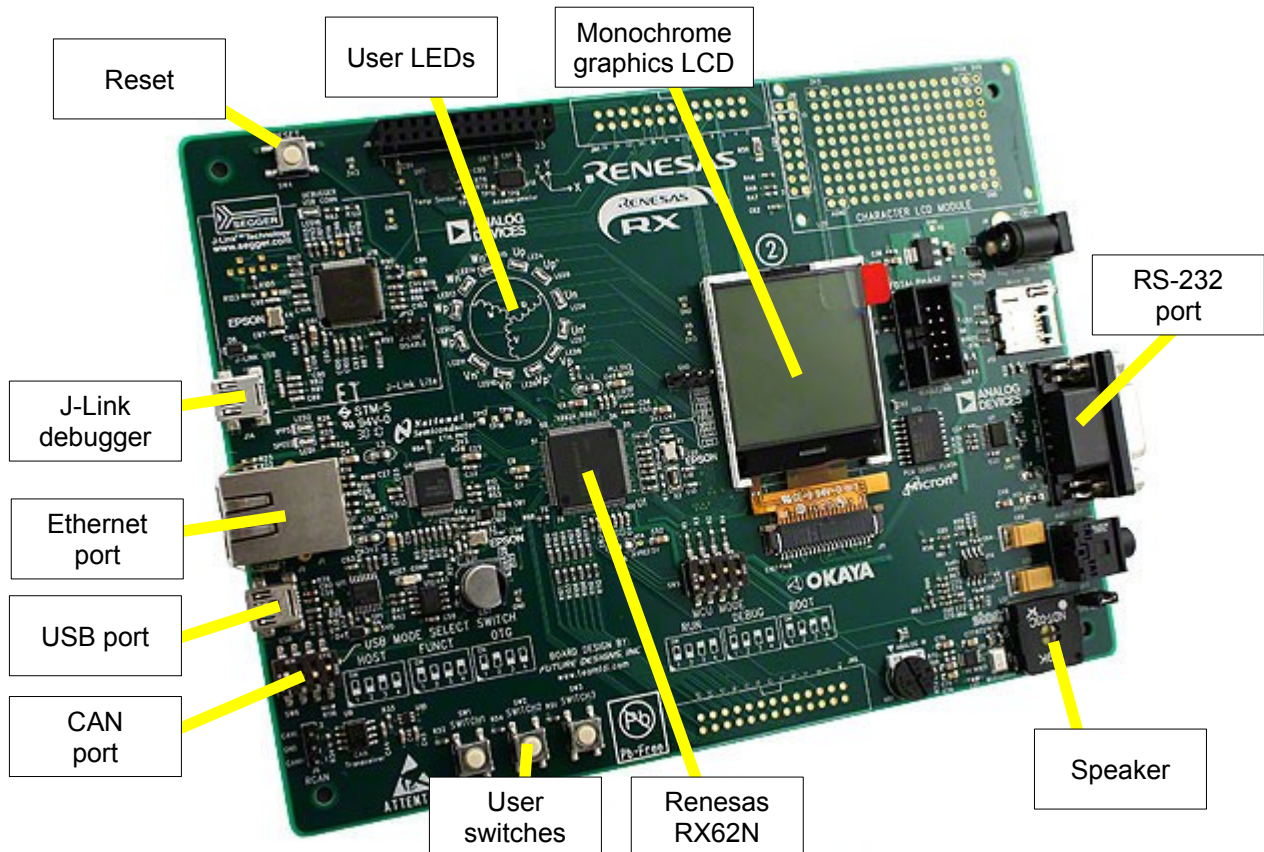
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# 1 Introduction

This QP Development Kit™ (QDK) describes how to use the QP/C™ and QP™/C++ state machine frameworks and the QM™ modeling tool for projects based on the Renesas RX family of 32-bit processors. This QDK uses the YRDKRX62N development board from Renesas shown in Figure 1 as well as the IAR EWRX toolset.

Figure 1: Renesas YRDKRX62N board



The actual hardware/software used to test this QDK is described below:

- Renesas YRDKRX62N Development Kit (see [Figure 1](#))
- IAR Embedded Workbench for Renesas RX KickStart edition version **2.30**
- QP/C or QP/C++ version **4.3.00** or higher.

**NOTE:** The Renesas YRDKRX62N evaluation kit comes with an installation CD with assorted software and utilities. This QDK requires nothing from the CD to be installed or used.

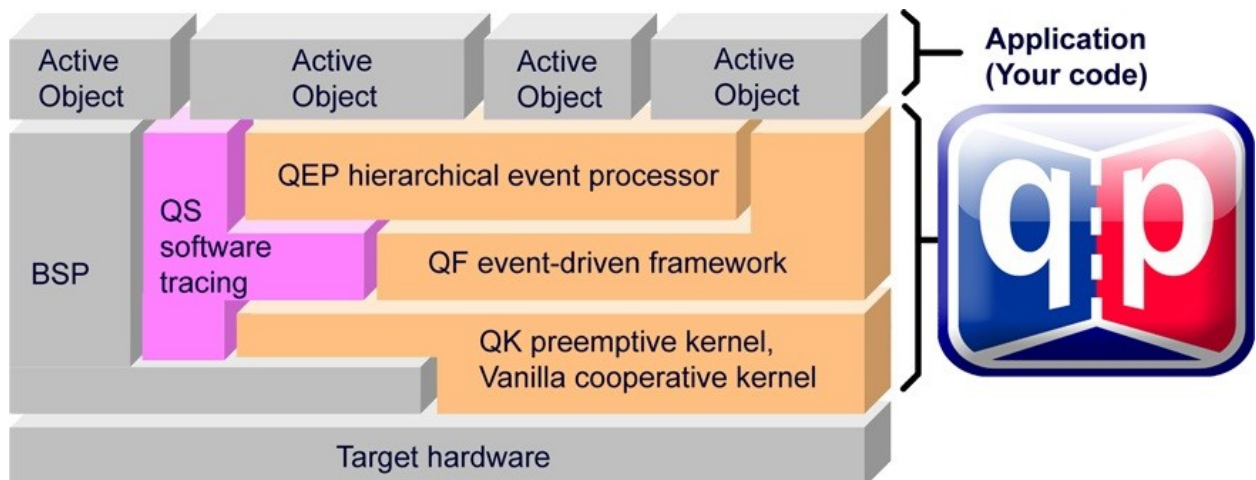
## 1.1 About QP™

QP™ is a family of very lightweight, open source, state machine-based frameworks for developing event-driven applications. QP enables building well-structured embedded applications as a set of concurrently executing hierarchical state machines (UML statecharts) directly in C or C++, or by means of the QM™ graphical UML modeling tool. QP is described in great detail in the book “*Practical UML Statecharts in C/C++, Second Edition: Event-Driven Programming for Embedded Systems*” [PSiCC2] (Newnes, 2008).

As shown in [Figure 2](#), QP consists of a universal UM-compliant event processor (QEP), a portable real-time framework (QF), a tiny run-to-completion kernel (QK) as well as simple cooperative kernel (Vanilla), and software tracing instrumentation (QS). Current versions of QP include: QP/C™ and QP/C++™, which require about 4KB of code and a few hundred bytes of RAM, and the ultra-lightweight QP-nano, which requires only 1-2KB of code and just several bytes of RAM. QP can manage up to 63 concurrently executing tasks structured as state machines (called active objects in UML).



**Figure 2: QP Components and their relationship with the target hardware, board support package (BSP), and the application**



## 1.2 About QM™

QM™ (QP™ Modeler) is a free, cross-platform, graphical UML modeling tool for designing and implementing real-time embedded applications based on the QP™ state machine frameworks. QM™ is available for Windows, Linux, and Mac OS X.

QM™ provides intuitive diagramming environment for creating good looking hierarchical state machine diagrams and hierarchical outline of your entire application. QM™ eliminates coding errors by automatic generation of compact C or C++ code that is 100% traceable from your design. Please visit [state-machine.com/qm](http://state-machine.com/qm) for more information about QM™.

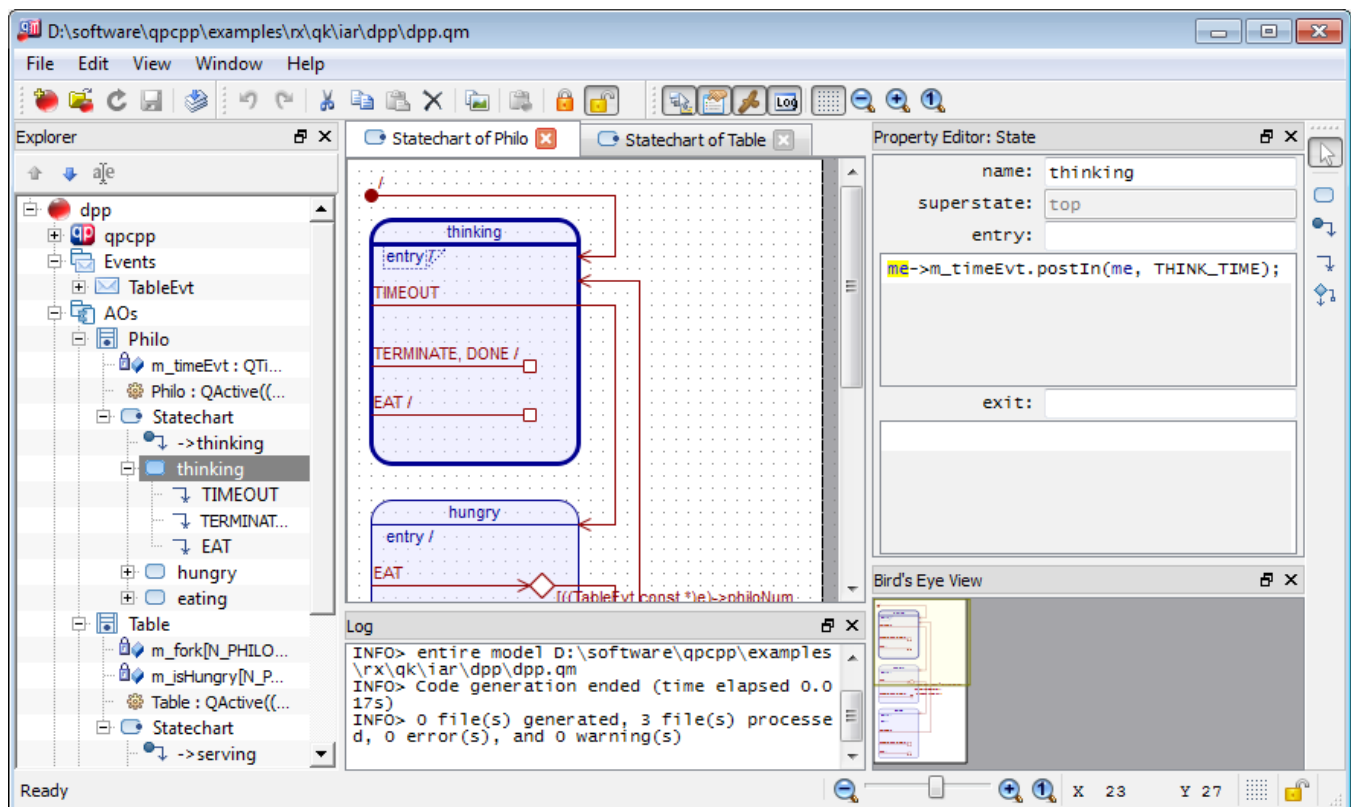


## 1.3 About this QDK-RX

This QDK provides working examples of code running under both the cooperative Vanilla kernel and the preemptive QK kernel. The example code is based on the Dining Philosopher Problem (DPP) sample application described in Chapter 7 of [PSiCC2] as well as in the Application Note “Dining Philosopher Problem” [QL AN-DPP 08] (included in the example code distribution).

The entire source code included with this QDK can be edited manually in a traditional code editor. However, significant parts of the code have been generated **automatically** by the QM™ modeling tool from the `dppp.qm` model file included in the QDK. The preferred way of developing QP™ applications is to make all the changes in the model and generate the code automatically.

Figure 3: The example model opened in the QM™ modeling tool



The QDK-RX example code includes the following components:

- Board support package (BSP) which provides interrupt service routines (ISRs), all QP callbacks, and an interface to the board's LEDs, push buttons, system clock tick timer, and serial port.
- QP port to RX for the Vanilla cooperative kernel described in Chapter 7 of [PSiCC2]
- QP port to RX for the preemptive run-to-completion QK kernel described in Chapter 10 of [PSiCC2]
- The DPP example for both the cooperative Vanilla kernel and the preemptive QK kernel.
- The QM™ model of the Dining Philosophers Problem (see [Figure 3](#))

---

**NOTE:** The significant parts of the source code (files `dpp.h`, `philo.c`, and `table.c`) have been generated by the QM™ modeling tool from the `dppp.qm` model, which is the same for the Vanilla and QK versions of the DPP application. These files can be edited by hand (after unchecking the read-only property), but the changes made at the code level won't be incorporated back into the model.

---

## 1.4 Licensing QP™

The **Generally Available (GA)** distribution of QP™ available for download from the [www.state-machine.com/downloads](http://www.state-machine.com/downloads) website is offered with the following two licensing options:

- The GNU General Public License version 2 (GPL) as published by the Free Software Foundation and appearing in the file `GPL.TXT` included in the packaging of every Quantum Leaps software distribution. The GPL *open source* license allows you to use the software at no charge under the condition that if you redistribute the original software or applications derived from it, the complete source code for your application must be also available under the conditions of the GPL (GPL Section 2[b]).
- One of several Quantum Leaps commercial licenses, which are designed for customers who wish to retain the proprietary status of their code and therefore cannot use the GNU General Public License. The customers who license Quantum Leaps software under the commercial licenses do not use the software under the GPL and therefore are not subject to any of its terms.

For more information, please visit the licensing section of our website at: [www.state-machine.com/licensing](http://www.state-machine.com/licensing)



## 1.5 Licensing QM™

The QM™ graphical modeling tool available for download from the [www.state-machine.com/downloads](http://www.state-machine.com/downloads) website is **free** to use, but is not open source. During the installation you will need to accept a basic End-User License Agreement (EULA), which legally protects Quantum Leaps from any warranty claims, prohibits removing any copyright notices from QM, selling it, and creating similar competitive products.



## 2 Getting Started

This section describes how to install, build, and use the QDK-RX-IAR. This section assumes that you have the YRDKRX62N board, and have downloaded and installed the IAR EWRX toolset on your machine. Also this section assumes that you have downloaded and installed the **QP™ Baseline Code**, available for a separate download from [www.state-machine.com/downloads](http://www.state-machine.com/downloads).

---

**NOTE:** To avoid repetitions, every QDK™ contains only the QP ports and example(s) pertaining to the specific MCU and compiler, but does not include the platform-independent baseline code of QP™, which is available for a separate download. It is strongly recommended that you read Chapter 12 in [PSiCC2] before you start with this QDK™. The QP directory structure is described in detail in a separate Quantum Leaps Application Note: “QP Directory Structure” [QL AN-Directory 07]).

**NOTE:** This QDK Manual pertains both to C and C++ versions of the QP™ state machine frameworks. Most of the code listings in this document refer to the QP/C version. Occasionally the C code is followed by the equivalent C++ implementation to show the C++ differences whenever such differences become important.

---

### 2.1 Installing the QDK-RX-IAR

The QDK code is distributed in a ZIP archive (`qdkc_rx-iar_yrdrx62n.zip` for QP/C and `qdkcpp_rx-iar_yrdrx62n.zip` for QP/C++). You need to unzip this archive into the same directory, into which you've installed QP. The following [Listing 1](#) shows the directory structure and selected files after you complete the QP and QDK-RX-IAR installation. (Please note that the QP directory structure is described in detail in a separate Quantum Leaps Application Note: “[QP Directory Structure](#)”).

**Listing 1: Selected directories and files after installing QP and the QDK-RX-IAR code.**  
**The boldface indicates directories and files included in the QDK.**

```

qpc/                                - QP installation directory
  +-doc\
  | +-AN_DPP.pdf                    - Application Note "Dining Philosopher Problem Example"
  | +-QDK_RX-IAR_YRDKRX62N.pdf      - This QDK Manual "QDK Renesas RX with IAR"
  |
  +-include\                         - QP platform-independent include files
  +-qep\                             - QEP platform-independent source code
  +-qf\                             - QF platform-independent source code
  +-qk\                             - QK platform-independent source code
  +-qs\                             - QS platform-independent source code
  |
  +-examples\                       - subdirectory containing the QP examples
  | +-rx\                           - Renesas RX examples
  | | +-vanilla\                   - Ports to the non-preemptive "vanilla" kernel
  | | | +-iar\                     - IAR compiler
  | | | | +-dpp-yrdrx62n\          - DPP example for (non-preemptive) for YRDKRX62N
  | | | | | +-Debug\              - directory containing the Debug build
  | | | | | | +-dpp.out            - image of the DPP application
  | | | | | +-Release\            - directory containing the Release build
  | | | | | +-Spy\                - directory containing the Spy build
  | | | | |
  | | | | | +-bsp.c                - BSP for the YRDKRX62N (non-preemptive)
  | | | | | +-bsp.h                - BSP header file
  | | | | | +-main.c              - the main function
  | | | | | +-dpp.h                - the DPP application header file

```



```

| | | | +-dpp.qm - QM model for the DPP application
| | | | +-dpp.ewp - IAR EWRX project for the DPP application
| | | | +-dpp.eww - IAR EWRX workspace for the DPP application
| | | | +-philos.c - the Philosopher active objects
| | | | +-table.c - the Table active object
| | | |
| | +-qk\ - Ports to the preemptive QK kernel
| | | +-iar\ - IAR compiler
| | | | +-dpp-qk-yrdkrx62n\ - DPP example for (preemptive) for YRDKRX62N
| | | | | +-Debug\ - directory containing the Debug build
| | | | | | +-dpp.out - image of the DPP application
| | | | | | +-dpp.map - map file of the DPP application
| | | | | +-Release\ - directory containing the Release build
| | | | | +-Spy\ - directory containing the Spy build
| | | | |
| | | | | +-bsp.c - BSP for the YRDKRX62N (preemptive)
| | | | | +-bsp.h - BSP header file
| | | | | +-main.c - the main function
| | | | | +-dpp.h - the DPP application header file
| | | | | +-dpp.qm - QM model for the DPP application
| | | | | +-dpp.ewp - IAR EWRX project for the DPP application
| | | | | +-dpp.eww - IAR EWRX workspace for the DPP application
| | | | | +-philos.c - the Philosopher active objects
| | | | | +-table.c - the Table active object
|
+-ports\ - subdirectory containing the QP ports
| +-rx\ - Renesas RX ports
| | +-vanilla\ - Ports to the non-preemptive "Vanilla" kernel
| | | +-iar\ - IAR compiler
| | | | +-dbg\ - Debug build
| | | | | +-libqep_RX600.a - QEP library for RX600 core
| | | | | +-libqf_RX600.a - QF library for RX600 core
| | | | +-rel\ - Release build
| | | | +-spy\ - Spy build
| | | | | +-libqep_RX600.a - QEP library for RX600 core
| | | | | +-libqf_RX600.a - QF library for RX600 core
| | | | | +-libqs_RX600.a - QS library for RX600 core
| | | | +-make_rx600.bat - Batch to build QP for RX600 core
| | | | +-qep_port.h - QEP platform-dependent public include
| | | | +-qf_port.h - QF platform-dependent public include
| | | | +-qp_port.h - QP platform-dependent public include
| | | | +-qs_port.h - QS platform-dependent public include
| | +-qk\ - QK (preemptive kernel) ports
| | | +-iar\ - IAR compiler
| | | | +-dbg\ - Debug build
| | | | | +-libqep_RX600.a - QEP library for RX600 core
| | | | | +-libqf_RX600.a - QF library for RX600 core
| | | | | +-libqk_RX600.a - QK library for RX600 core
| | | | +-rel\ - Release build
| | | | +-spy\ - Spy build
| | | | +-make_rx600.bat - Batch to build QP for RX600 core
| | | | +-qep_port.h - QEP platform-dependent public include
| | | | +-qf_port.h - QF platform-dependent public include
| | | | +-qk_port.h - QK platform-dependent public include
| | | | +-qp_port.h - QP platform-dependent public include
| | | | +-qs_port.h - QS platform-dependent public include

```

## 2.2 Building the QP™ Libraries

All QP components are deployed as libraries that you statically link to your application. The pre-built libraries for QEP, QF, QS, and QK are provided inside the `<qp>\ports\rx\` directory, so you don't need to build the QP libraries if you use the same toolset and the standard QP configuration. This section describes steps you need to take to rebuild the libraries yourself.

---

**NOTE:** To achieve commonality among different development tools, Quantum Leaps software does not use the vendor-specific IDEs, such as the IAR EWRX, for building the QP libraries. Instead, QP supports *command-line* build process based on simple batch scripts.

---

The code distribution contains the batch file `make_<core>.bat` for building all the libraries located in the `<qp>\ports\rx\...` directory. For example, to build the debug version of all the QP libraries for the RX600 core with the IAR compiler, QK kernel, you open a console window on a Windows PC, change directory to `<qp>\ports\rx\qk\iar\`, and invoke the batch by typing at the command prompt the following command:

```
make_rx600
```

The build process should produce the QP libraries in the location: `<qp>\ports\rx\qk\iar\dbg\`. The `make_rx600.bat` files assume that the IAR EWRX toolset has been installed in the directory `C:\tools\IAR\RX_KS_2.30\`. You need to adjust the symbol `IAR_RX` at the top of the batch script if you've installed the IAR RX compiler into a different directory.

---

**NOTE:** The QP libraries and QP applications can be built in the following three **build configurations**:

**Debug** - this configuration is built with full debugging information and minimal optimization. When the QP framework finds no events to process, the framework busy-idles until there are new events to process.

**Release** - this configuration is built with no debugging information and high optimization. Single-stepping and debugging is effectively impossible due to the lack of debugging information and optimized code, but the debugger can be used to download and start the executable. When the QP framework finds no events to process, the framework puts the CPU to sleep until there are new events to process.

**Spy** - like the debug variant, this variant is built with full debugging information and minimal optimization. Additionally, it is built with the QP's Q-SPY trace functionality built in. The on-board serial port and the Q-Spy host application are used for sending and viewing trace data. Like the Debug configuration, the QP framework busy-idles until there are new events to process.

---

In order to take advantage of the QS ("spy") instrumentation, you need to build the QS configuration of the QP libraries. You achieve this by invoking the `make_rx600.bat` utility with the "spy" target, like this:

```
make_rx600 spy
```

The make process should produce the QP libraries in the directory: `<qp>\ports\rx\qk\iar\spy\`.

You choose the build configuration by providing a target to the `make_rx600.bat` script. The default target is "dbg". Other targets are "rel", and "spy", respectively.

**Table 1: Building QP libraries for the Debug, Release, and Spy software configurations**

Software Version	Build command
Debug (default)	<code>make_rx600</code>
Release	<code>make_rx600 rel</code>
Spy	<code>make_rx600 spy</code>

## 2.3 Building the Examples

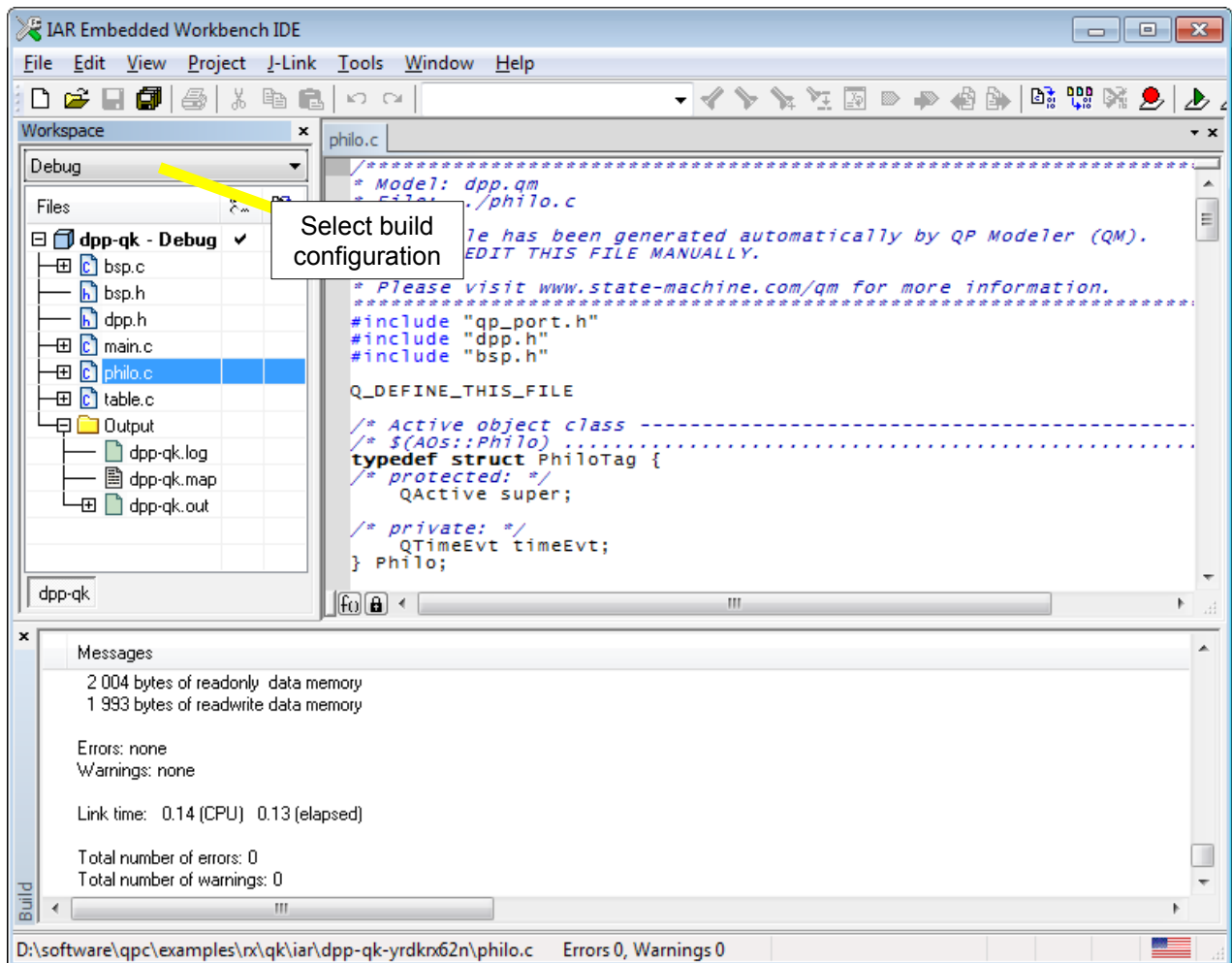
The examples accompanying this QDK-RX-IAR are based on the DPP application (see Quantum Leaps Application Note: “Dining Philosophers Problem Application” [QL AN-DPP 08] included in this QDK). The example directory `qpc\examples\rx\` contains the IAR workspaces and project that you can load into the IAR EWRX IDE, as shown in Figure 4.

For example, to build the DP example for the QK preemptive kernel perform the following steps:

- Launch IAR EWRX and open the project `dpp-qk.eww` (located in `qpc\examples\rx\qk\iar\dpp-qk-yrdkrx62n\`)
- Build the project by select Project|Build menu or by pressing F7. The project file contains three build configurations Debug, Release, and Spy. You can select the build configuration by means of the drop-down list on the IAR toolbar, as shown in Figure 4.

**NOTE:** The provided IAR project file assumes that the environment variable **QPC** has been defined to point to the directory, where the QP/C framework has been installed. (You should define the environment variable **QPCPP** for the QP/C++ framework).

Figure 4: IAR EWRX IDE with the DPP example project



## 2.4 Running the Examples

You program the code into the flash memory of the MCU through the IAR EWRX IDE by selecting Project | Download and Debug option. You run the program by selecting the Debug | Run menu (F5), or by clicking on the Run button.

After you download the code, the IAR C-SPY debugger will stop the program at `main()`. Please press Go to let the program continue. The User LEDs of the YRDKRX62N board should start blinking (see [Figure 1](#)). The LEDs are assigned as follows: LED4, LED5, LED6, LED7, and LED8 show the status of Dining Philosophers 0-4, respectively. These LEDs are on when the corresponding Philosopher is in the “eating” state, otherwise the LEDs are off.

The User LED12 is used to visualize the idle loop activity. The brightness of the LED12 is proportional to the frequency of invocations of the idle loop. The LED12 is always toggled with interrupts disabled, so no interrupt execution time contributes to the brightness of the User LED12.

The LCD display is not used in the DPP example, even though the backlight of the LCD is on. On the YRDKRX62N board the LCD backlight is hard-wired and is not controlled by the MCU, so it cannot be turned off.

### 2.4.1 Q-SPY Software Tracing

QS is a software tracing facility built into all QP components and also available to the Application code. QS allows you to gain unprecedented visibility into your application by selectively logging almost all interesting events occurring within state machines, the framework, the kernel, and your application code. QS software tracing is minimally intrusive, offers precise time-stamping, sophisticated runtime filtering of events, and good data compression (see Chapter 11 in [PSiCC2]).

To see the QS software trace output, you need to connect the RS-232 Port of the YRDKRX62N board (see [Figure 1](#)) to the COM port of your PC with a straight-through RS-232 cable. Alternatively, you can use an RS-232-to-USB converter connected directly to the RS-232 Port of the YRDKRX62N board.

In the IAR IDE you need to switch to the Spy configuration and download it to the target board. Next you need to launch the QSPY host utility in the Windows console to observe the output in the human-readable format.

---

**NOTE:** The QSPY host utility is part of the **Qtools** collection, available for download from <http://www.state-machine.com/downloads/index.php#QTools>. After installing Qtools, you should add the installation directory to the PATH environment variable.

---

You launch the QSPY utility on a Windows PC :

```
qspy -c COM9
```

This will start the QSPY host application to listen on COM2 serial port with the standard baud rate 115200. (Please use the actual virtual COM port number on your PC.) The screen shot in [Figure 5](#) shows the QSPY output from the DPP run:

Figure 5: Screen shot from the QSPY run

```

Administrator: Command Prompt
TICK : Ctr= 25
0000046876 QK_sche: prio= 5, pin= 0
0000046876 Disp==>: Obj=1_philo[4] Sig=TIMEOUT_SIG Active=Philo::thinking
0000046878 QK_sche: prio= 6, pin= 5
0000046878 Disp==>: Obj=1_table Sig=HUNGRY_SIG Active=Table::serving
0000046879 User000: 4 hungry
0000046881 User000: 4 eating
0000046882 Intern: Obj=1_table Sig=HUNGRY_SIG Source=Table::serving
Q_ENTRY: Obj=1_philo[4] State=Philo::hungry
0000046884 ==>Tran: Obj=1_philo[4] Sig=TIMEOUT_SIG Source=Philo::thinking New=Philo::hungry
0000046885 QK_sche: prio= 5, pin= 0
0000046885 Disp==>: Obj=1_philo[4] Sig=EAT_SIG Active=Philo::hungry
Q_ENTRY: Obj=1_philo[4] State=Philo::eating
0000046887 ==>Tran: Obj=1_philo[4] Sig=EAT_SIG Source=Philo::hungry New=Philo::eating
0000046888 QK_sche: prio= 4, pin= 0
0000046889 Disp==>: Obj=1_philo[3] Sig=TIMEOUT_SIG Active=Philo::thinking
0000046890 QK_sche: prio= 6, pin= 4
0000046891 Disp==>: Obj=1_table Sig=HUNGRY_SIG Active=Table::serving
0000046892 User000: 3 hungry
0000046893 Intern: Obj=1_table Sig=HUNGRY_SIG Source=Table::serving
Q_ENTRY: Obj=1_philo[3] State=Philo::hungry
0000046894 ==>Tran: Obj=1_philo[3] Sig=TIMEOUT_SIG Source=Philo::thinking New=Philo::hungry
0000046896 QK_sche: prio= 4, pin= 0
0000046896 Disp==>: Obj=1_philo[3] Sig=EAT_SIG Active=Philo::hungry
0000046897 Ignored: Obj=1_philo[3] Sig=EAT_SIG Active=Philo::hungry
0000046898 QK_sche: prio= 3, pin= 0
0000046899 Disp==>: Obj=1_philo[2] Sig=TIMEOUT_SIG Active=Philo::thinking
0000046900 QK_sche: prio= 6, pin= 3
0000046901 Disp==>: Obj=1_table Sig=HUNGRY_SIG Active=Table::serving
0000046902 User000: 2 hungry
0000046904 User000: 2 eating
0000046904 Intern: Obj=1_table Sig=HUNGRY_SIG Source=Table::serving
0000046905 QK_sche: prio= 5, pin= 3
0000046906 Disp==>: Obj=1_philo[4] Sig=EAT_SIG Active=Philo::eating
0000046907 Intern: Obj=1_philo[4] Sig=EAT_SIG Source=Philo::eating
0000046908 QK_sche: prio= 4, pin= 3
0000046909 Disp==>: Obj=1_philo[3] Sig=EAT_SIG Active=Philo::hungry
0000046909 Ignored: Obj=1_philo[3] Sig=EAT_SIG Active=Philo::hungry
Q_ENTRY: Obj=1_philo[2] State=Philo::hungry
0000046911 ==>Tran: Obj=1_philo[2] Sig=TIMEOUT_SIG Source=Philo::thinking New=Philo::hungry
0000046912 QK_sche: prio= 3, pin= 0
0000046913 Disp==>: Obj=1_philo[2] Sig=EAT_SIG Active=Philo::hungry
0000046914 Ignored: Obj=1_philo[2] Sig=EAT_SIG Active=Philo::hungry
0000046915 QK_sche: prio= 3, pin= 0
0000046915 Disp==>: Obj=1_philo[2] Sig=EAT_SIG Active=Philo::hungry
Q_ENTRY: Obj=1_philo[2] State=Philo::eating
0000046917 ==>Tran: Obj=1_philo[2] Sig=EAT_SIG Source=Philo::hungry New=Philo::eating
0000046918 QK_sche: prio= 2, pin= 0
0000046919 Disp==>: Obj=1_philo[1] Sig=TIMEOUT_SIG Active=Philo::thinking
0000046920 QK_sche: prio= 6, pin= 2
0000046921 Disp==>: Obj=1_table Sig=HUNGRY_SIG Active=Table::serving
0000046922 User000: 1 hungry
0000046923 Intern: Obj=1_table Sig=HUNGRY_SIG Source=Table::serving
Q_ENTRY: Obj=1_philo[1] State=Philo::hungry
0000046924 ==>Tran: Obj=1_philo[1] Sig=TIMEOUT_SIG Source=Philo::thinking New=Philo::hungry
  
```

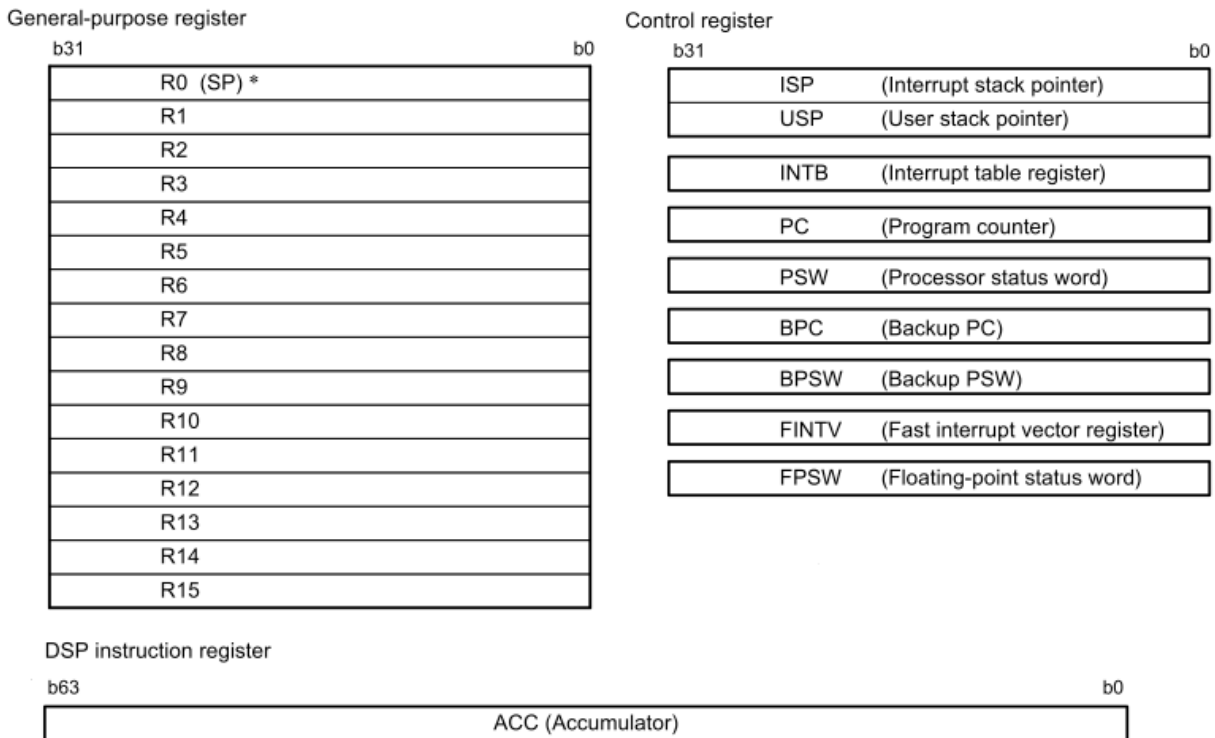
### 3 The Renesas RX CPU

This section provides a very quick overview of the Renesas RX CPU and its features relevant to the QP framework.

#### 3.1 RX CPU Register Set

The RX CPU has sixteen general-purpose 32-bit registers, nine 32-bit control registers, and one 64-bit accumulator used for DSP instructions.

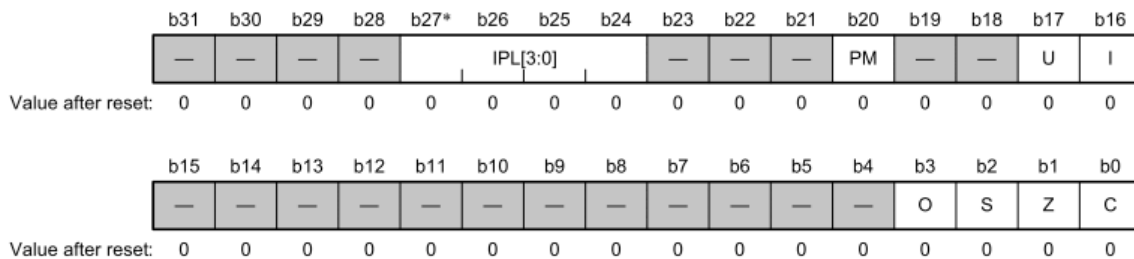
**Figure 6: RX CPU register set**



##### 3.1.1 The Processor Status Word (PSW) Register

The 32-bit Processor Status Word (PSW) register (see Figure 7) deserves some extra attention.

**Figure 7: RX Processor Status Word (PSW) register**



Note : \* Since the interrupt priority levels are from 0 to 7 for the RX610 Group, bit 27 is reserved. Writing to bit 27 is ineffective.

The PSW has an interrupt control bit (PSW[I], bit 16) that globally enables (PSW[I] = 1) or disables (PSW[I] = 0) interrupts. Furthermore, a 4-bit field called Interrupt Priority Level (PSW[IPL], bits 24-27) reflects the current interrupt priority level. All interrupts to the CPU are assigned a priority of 0-15, with 0 being the lowest priority, and 15 being the highest priority. When PSW[I] = 1 (interrupts are enabled), any interrupt with a priority higher than the current IPL will interrupt the CPU. Interrupts of a priority less than or equal to the current IPL value are kept pending until the IPL drops.

---

**NOTE:** The RX610 series only has a 3-bit IPL field (values 0-7); bit 27 is reserved, writes are ignored. At reset, PSW[I] = 0 (interrupts disabled) and PSW[IPL] = 0 (lowest priority level).

---

### 3.2 RX CPU Modes

The RX CPU supports two processor modes: Supervisor and User. Each processor mode imposes a level on rights of access to memory and the instructions that can be executed. Supervisor mode carries greater rights than user mode and this initial mode out of reset. **All QP ports to RX CPU run exclusively in the Supervisor mode.**

### 3.3 RX CPU Stacks

The RX stack pointer (R0) can be either the interrupt stack pointer (ISP) or the user stack pointer (USP), depending on the value of the stack pointer select bit (U) in the processor status word (PSW). **All QP ports to RX CPU use exclusively the interrupt stack pointer (ISP)** and the user stack pointer is not used at all. Consequently, the user stack size should be set to zero to prevent wasting of RAM (see also [Figure 9](#)).

### 3.4 RX CPU Interrupt Processing (Hardware)

The RX family features a sophisticated interrupt control unit (ICU) and a prioritized hardware interrupt scheme that is a perfect fit for the QP's single-stack, run-to-completion execution architecture. [Figure 8](#) shows the parts of the exception processing handled automatically by the hardware and the parts handled by the software.

As shown in [Figure 8](#), the hardware processing includes the following steps executed **atomically**:

1. The exception is acknowledged/accepted by the processor
2. The processor status word (PSW) is stacked automatically
3. PSW[I] is cleared, **disabling interrupts**

---

**NOTE:** The RX processor disables interrupts automatically and atomically in hardware as part of the interrupt entry sequence.

---

4. The program counter (PC) of the next instruction (after returning from interrupt) is stacked automatically
5. PSW[IPL] is set to the priority of the current interrupt
6. The PC is loaded with the vector from the vector table, and execution of the service routine begins

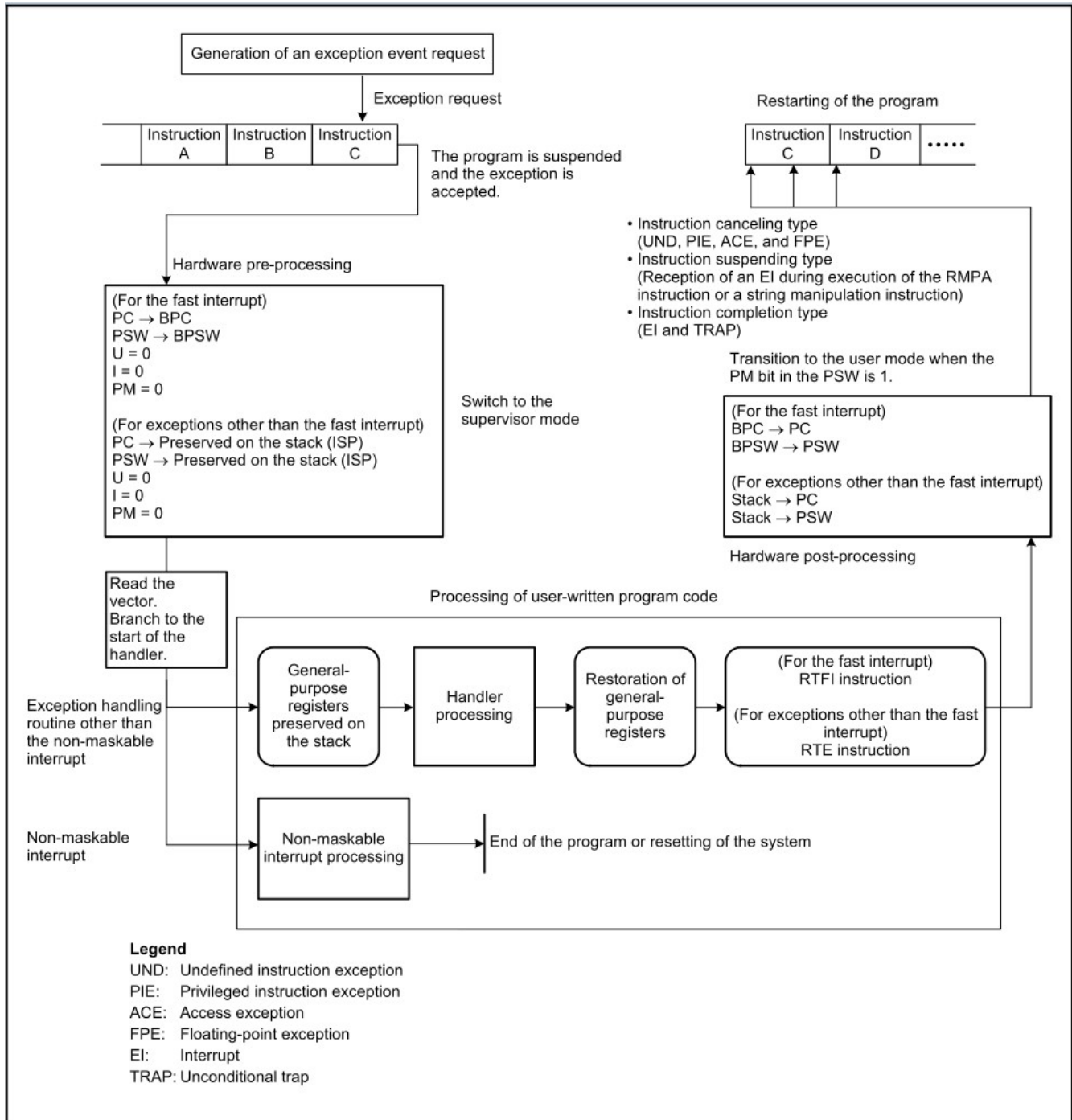
---

**NOTE:** The RX processor supports also the concept of a **fast interrupt**, which uses the backup PC (BPC) and the backup PSW (BPSW) registers instead of the stack for preserving the PC and the PSW, respectively.

The fast interrupt can be used with the cooperative "Vanilla" kernel, but should **not be used with the preemptive QK kernel**, because it does not use the machine's natural stack protocol.

---

**Figure 8: RX exception processing**



After vectoring to the Interrupt Service Routine (ISR), the software takes over (see the next section). The software returns from the ISR by executing the RTE instruction (or RTFI for the fast interrupt), at which point the hardware takes over and executes the hardware post processing. This **atomic** sequence consists of restoring the PSW and PC from the stack and resuming the interrupted program.

### 3.5 RX CPU Interrupt Processing (Software)

The IAR C/C++ RX compiler, as most embedded cross-compilers, can generate interrupt service routines (ISRs), which are designated with the special extended keyword `__interrupt` (see Listing 2). The IAR compiler can also automatically populate the RX vector table with the address of the ISR, when you provide the vector number by means of the `#pragma vector` declaration.

**Listing 2: Defining an interrupt function with IAR compiler**

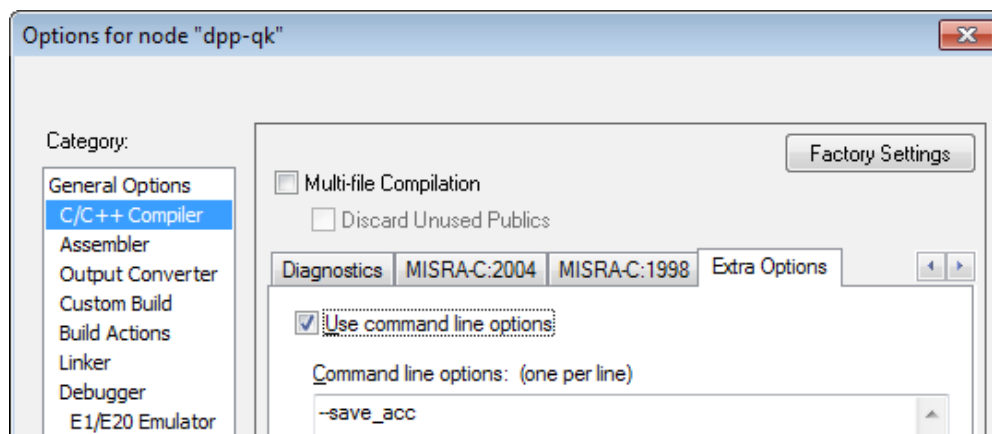
```
#pragma vector = 28 /* Vector number from in I/O header file */
__interrupt void MyInterruptRoutine(void) {
    /* Do something */
}
```

**NOTE:** An interrupt function must have the return type void, and it cannot specify any parameters.

In case of the RX processor, such compiler-generated ISRs are perfectly suitable for the QP framework (including both the cooperative “Vanilla” kernel and the preemptive QK kernel), but in case of the QK kernel special care must be taken to preserve all the registers possibly used by the tasks. Also, for any kind of kernel, you need to understand which registers are and, more importantly, aren’t saved and restored by the compiler, so that you know which operations are **not** allowed in the ISR code.

By default, the IAR `__interrupt` function saves and restores any general-purpose registers clobbered by this function and returns with the `RTE` instruction. However, the interrupt function does **not** save the Accumulator or the `FPSW` registers. This means that the ISR cannot perform any operations that clobber the Accumulator or the `FPSW` register, such as the multiply, multiply-and-accumulate instructions; `EMUL`, `EMULU`, `FMUL`, `MUL`, and `RMPA`, or any floating-point instructions in which case the prior value in the accumulator and/or the `FPSW` register is modified by execution of the instruction.

The IAR compiler provides the `--save_acc` command-line option to enforce saving and restoring the 64-bit Accumulator register in the `__interrupt` functions. In the IAR EWRX IDE, this option needs to be specified in the “Extra Options” tab, as shown below:



**NOTE:** The `--save_acc` option **must** be specified for all QK projects and all “Vanilla” kernel projects that can clobber the Accumulator in the ISRs.

**NOTE:** In any case (with or without the `--save_acc` option) the ISR **cannot** use any floating-point instructions.

## 4 Non-Preemptive “Vanilla” Port

The “Vanilla” port shows how to use the QP frameworks on an RX-based system with the non-preemptive “Vanilla” kernel. In this version you’re using the cooperative kernel built-into the QF framework and you’re not using the QK component.

---

**NOTE:** The source code for the QP port to the cooperative “Vanilla” kernel is generic and should not need to change for different members of the Renesas 32-Bit MCU RX Family (RX200, RX600, etc.).

---

### 4.1 The `qep_port.h` Header File

The QEP header file for the RX port is located in `qpc\ports\rx\vanilla\iar\qep_port.h`. Listing 3 shows the `qep_port.h` header file.

**Listing 3: `qep_port.h` header file for the non-preemptive QP configuration and IAR compiler**

```
(1) #include <stdint.h>          /* exact-width integers, WG14/N843 C99, 7.18.1.1 */
    #include "qep.h"            /* QEP platform-independent public interface */
```

- (1) The IAR Compiler provides the C99-standard exact-width integer types in the standard `<stdint.h>` header file.

### 4.2 The `qf_port.h` Header File

The QF port header file for the RX family is located in `qpc\ports\rx\vanilla\iar\qf_port.h`. This file specifies the configuration constants for QF (see Chapter 8 in [PsiCC2]) as well as the unconditional interrupt disabling/enabling and the critical section policy.

The most important porting decision you need to make in the `qf_port.h` header file is the critical section policy. The RX family of MCUs allows using the simplest “unconditional interrupt unlocking” policy (see Section 7.3.2 of [PsiCC2]), because RX

**Listing 4: `qf_port.h` header file for the non-preemptive QP configuration and IAR compiler**

```

/* The maximum number of active objects in the application */
(1) #define QF_MAX_ACTIVE          63
/* The maximum number of event pools in the application */
(2) #define QF_MAX_EPOOL          6
/* QF interrupt disabling/enabling */
(3) #define QF_INT_DISABLE()      __disable_interrupt()
(4) #define QF_INT_ENABLE()       __enable_interrupt()

/* QF critical section entry/exit */
(5) /* QF_CRIT_STAT_TYPE not defined: unconditional interrupt unlocking, NOTE01 */
(6) #define QF_CRIT_ENTRY(dummy)  __disable_interrupt()
(7) #define QF_CRIT_EXIT(dummy)   __enable_interrupt()

/* QF ISR entry/exit, also see NOTE01 */
(8) #define QF_ISR_ENTRY()        __enable_interrupt()
(9) #define QF_ISR_EXIT()         __disable_interrupt()

```

```
(10) #include <intrinsics.h> /* IAR intrinsic functions */  
  
#include "qep_port.h" /* QEP port */  
(11) #include "qvanilla.h" /* "Vanilla" cooperative kernel */  
#include "qf.h" /* QF platform-independent public interface */
```

- (1) The `QF_MAX_ACTIVE` macro specifies the maximum number of active object priorities in the application. You always need to provide this constant. Here, `QF_MAX_ACTIVE` is set to the maximum limit of 63 active object priorities in the system. You can decrease this number to reduce the RAM footprint of the QF framework.
- (2) The `QF_MAX_EPOOL` macro specifies the maximum number of event pools in the application.
- (3) The `QF_INT_DISABLE()` macro resolves to the intrinsic IAR function `__disable_interrupt()`, which in turn generates the "CLRPSW I" instruction. This single instruction clears PSW[I] in the PSW register, thereby disabling all interrupts.
- (4) The `QF_INT_ENABLE()` macro resolves to the intrinsic IAR function `__enable_interrupt()`, which in turn generates the "SETPSW I" instruction. This single instruction sets PSW[I] in the PSW register, thereby enabling all interrupts.
- (5) The `QF_CRIT_STAT_TYPE` macro is not defined, which means that the simple critical section policy of "unconditional interrupt locking and unlocking" is applied.
- (6) The `QF_CRIT_ENTRY()` macro does not use its parameter in this case and simply unconditionally disables interrupts.
- (7) The `QF_CRIT_EXIT()` macro does not use its parameter in this case and simply unconditionally re-enables interrupts.

---

**NOTE:** The simple and very efficient critical section policy **does not allow nesting** of critical sections. However, the RX interrupt handlers disable interrupts upon entry, so the body of the ISR becomes a critical section. To avoid nesting of critical sections, interrupts must be enabled before calling any QP service from an ISR. This enabling interrupts after entry to the ISR and disabling interrupts before exit is accomplished in the macros `QF_ISR_ENTRY()`/`QF_ISR_EXIT()` described below.

---

- (8) To avoid nesting of critical sections, the macro `QF_ISR_ENTRY()` must be called at the beginning of every ISR before invoking any QP services. This macro re-enables interrupts (i.e., permit interrupt nesting and preemption of the current ISR by higher-priority interrupts). Please note, however that the prioritized interrupt controller of the RX CPU prevents any interrupts of lower or equal priority from preempting the currently serviced interrupt level.

---

**NOTE:** If you don't wish interrupts to be able to preempt each other, you can always assign the same priorities to all interrupts.

---

- (9) the macro `QF_ISR_EXIT()` must be used at the very end of every ISR. This restores the CPU's PSW[I] bit to 0, just as it was when the ISR was entered.
- (10) The IAR header file `<intrinsics.h>` declares the prototypes of the interrupt locking/unlocking functions.
- (11) This QF port uses the cooperative "vanilla" kernel.

### 4.3 The Board Support Package for the “Vanilla” Port

The Board Support Package (BSP) for a QP application implements the board initialization, ISRs, QP callback functions, and application-specific board-specific functions. The whole BSP is located in the file `bsp.c` in the directory `qpc\examples\rx\vanilla\iar\dpp-yrdkrx62n\`.

#### 4.3.1 The Default Interrupt Handler

By default, the IAR startup code populates the RX vector table with a **default interrupt handler**. This means that each interrupt source without an explicit ISR vectors to the default interrupt handler.

The IAR toolset allows you to customize the behavior of the default interrupt handler by defining the `__exit()` function. The following listing shows the custom exit code that causes assertion failure, so it boils down to the common error handling policy of QP. The QP assertion failure callback is discussed in the upcoming section “Assertion Failure Callback”.

**Listing 5: The custom exit code called by the Default Interrupt Handler**

```
void __exit(int status) {
    (void)status; /* to avoid the compiler warning about unused parameter */
    Q_ERROR();
}
```

#### 4.3.2 Interrupt Service Routines (ISRs) for the “Vanilla” kernel

As mentioned earlier, the IAR toolset enables the user to write ISRs as interrupt functions in C/C++. These compiler-generated ISRs are perfectly adequate for the non-preemptive Vanilla kernel.

**Listing 6: Tick timer ISR for the Vanilla kernel in bsp.c**

```
(1) #pragma vector=28
(2) static __interrupt void tickISR(void) {
(3)     QF_ISR_ENTRY(); /* inform the QF vanilla kernel about entering the ISR */

(4) #ifdef Q_SPY
(5)     l_tickTime_ += l_tickPeriod; /* account for the clock rollover */
    #endif

(6)     QF_TICK(&l_tickISR); /* process all armed time events */

(7)     QF_ISR_EXIT(); /* inform the QF vanilla kernel about exiting the ISR */
}
```

- (1) The `#pragma` directs the IAR compiler to allocate the following interrupt function to the given vector.
- (2) The ISR is defined in C by means of the `__interrupt` extended keyword of the IAR compiler.
- (3) The macro `QF_ISR_ENTRY()` leaves the critical section established automatically by the RX hardware upon the entry to the interrupt. This allows calling the QP services (such as `QF_TICK()`) outside the critical section.
- (4) This code is conditionally compiled into the build when the macro `Q_SPY` is defined. When using QS the variable `l_tickTime_` keeps track of how many have elapsed so far. At the time an actual time-stamp is needed, the free running counter is added to this value to get a high resolution 32-bit time-stamp.

- (5) The macro `QF_TICK()` is used to notify the framework about another clock tick. This allows the framework to perform time-event management activities. This call may result in one or more events being posted to active objects which had started timers. The parameter to `QF_TICK()` is only used when tracing with QSPY, otherwise it is ignored.
- (6) The macro `QF_ISR_EXIT()` re-establishes again the critical section by restoring `PSW[I]` to the value it was upon first entering the ISR.

### 4.3.3 Idle loop customization in the Vanilla port

As described in Chapter 7 of [PSiCC2], when no events are available, the non-preemptive Vanilla scheduler invokes the platform-specific callback function `QF_onIdle()`, which you can use to save CPU power, or perform any other idle processing (such as Q-SPY software trace output).

---

**NOTE:** The idle callback `QF_onIdle()` must be invoked with interrupts disabled, because the idle condition can be changed by any interrupt that posts events to event queues. `QF_onIdle()` must internally unlock interrupts, ideally atomically with putting the CPU to the power-saving mode (see also Chapter 7 in [PSiCC2]).

---

#### Listing 7: Idle callback `QF_onidle()` for the Vanilla kernel in `bsp.c`

```
(1) void QF::onIdle(void) {                                     // entered with interrupts DISABLED
(2)     BSP_LED_IDLE_ON();                                     // toggle the User LED on and then off, see NOTE02
(3)     BSP_LED_IDLE_OFF();
(4) #ifdef Q_SPY
(5)     . . .
(6)     __wait_for_interrupt();
(7) #else
(8)     QF_INT_ENABLE();
    #endif
}
```

- (1) This routine is always entered with interrupts disabled to avoid a race condition with interrupts that could post one or more events to active objects and thus invalidate the idle condition.
- (2-3) The idle LED (LED12 of the YRDKRX62N board) is toggled on and off each time through the idle callback. Thus, a brighter LED indicates more idle time. A heavily loaded CPU will spend little or no time in the idle loop and thus the idle LED would be dim. Note that in a release build, the CPU will sleep most of the time, and the LED will be toggled only at the rate of the interrupts that wake up the CPU. In a debug build variant, the CPU never sleeps, and the LED's intensity gives a good indication of the idle task activity.
- (4) The software-tracing code is conditionally compiled into the build when enabled at compile time. When using QS, the trace data is sent out during idle loop processing. If the UART's Transmit Data Register (TDR) is empty, this code calls a QSPY API to see if there is another byte of data to send out the serial port.
- (5) In release mode (no debugger) the CPU can be put to low-power sleep.
- (6) The `__wait_for_interrupt()` intrinsic provided by the IAR compiler simply inserts a `WAIT` instruction to the RX CPU. (More advanced power management could be performed here; this port only sleeps the CPU, and does not put any other peripheral in low-power mode).

---

**NOTE:** Even though the WAIT instruction is executed with interrupts locked (PSW[I] = 0), the instruction re-enables interrupts (PSW[I] = 1) as the CPU goes to sleep. Thus, when the CPU re-wakes, interrupts are already enabled.

---

- (7) release build variant) or doing QSPY tracing, simply unlock interrupts (a requirement) before returning.

#### 4.3.4 Assertion-Failure Callback

As described in Chapter 6 of [PSiCC2], all QP components use internally assertions to detect errors in the way application is using the QP services. You need to define how the application reacts in case of assertion failure by providing the callback function `Q_onAssert()`. Typically, you would put the system in a fail-safe state and try to reset. It is also a good idea to log some information as to where the assertion failed.

The following listing shows the `Q_onAssert()` callback in the `bsp.c` file. The function disables all interrupts and hangs in an endless loop. When executing the code from a debugger you can break into the code and inspect the cause of the assertion by backtracking the call stack.

---

**NOTE:** This policy is only adequate for testing, but is **not** adequate for production release.

---

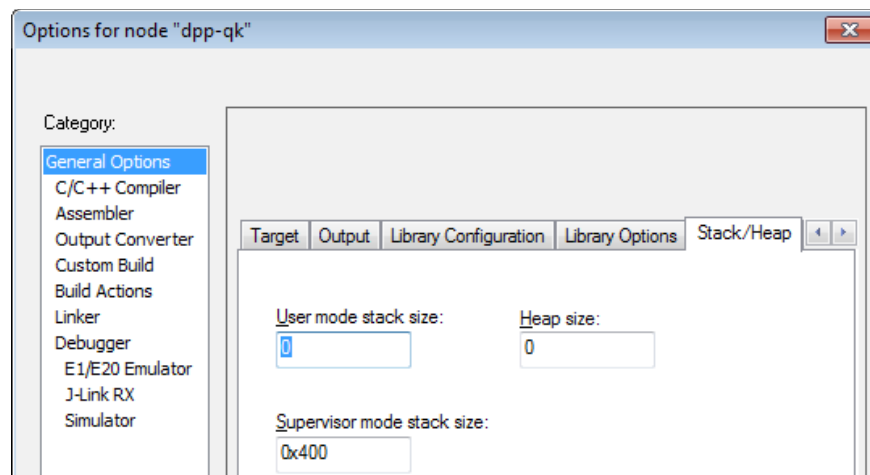
##### Listing 8: Assertion-Failure callback in bsp.c

```
void Q_onAssert(char const Q_ROM * const Q_ROM_VAR file, int line) {
    (void) file; /* avoid compiler warning */
    (void) line; /* avoid compiler warning */
    QF_INT_DISABLE();
    for (;;) {
    }
}
```

#### 4.3.5 Specifying the Stacks

As described before, the QP framework uses exclusively the Supervisor stack and does not use the User Stack at all. Consequently, you should set the User stack to zero. The following screen shot shows how to accomplish this in the IAR IDE. In the project General Options, select the Stack/Heap tab.

**Figure 9: Setting the size of stacks and heap in the IAR IDE**



## 5 Preemptive QK Port

This section describes how to use QP with the preemptive QK real-time kernel described in Chapter 10 of [PsiCC2]. The benefit is very fast, fully deterministic task-level response and that execution timing of the high-priority tasks (active objects) will be virtually insensitive to any changes in the lower-priority tasks. The downside is bigger RAM requirement for the stack. Additionally, as with any preemptive kernel, you must be very careful to avoid any sharing of resources among concurrently executing active objects, or if you do need to share resources, you need to protect them with the QK priority-ceiling mutex (again see Chapter 10 of [PsiCC2]).

---

**NOTE:** The preemptive configuration with QK uses more stack than the non-preemptive Vanilla configuration. You may need to adjust the Supervisor mode stack size to be large enough for your application.

---

As mentioned earlier, the RX family's interrupt control and handling is a perfect match for a single-stack run-to-completion kernel. As in the Vanilla kernel, also under the QK kernel the CPU executes in Supervisor Mode using the Interrupt Stack Pointer. User Mode, and the User Stack Pointer, are unused.

As with the Vanilla port, the QK allows nested interrupts by (re-)enabling interrupts inside ISRs once it is safe. It is the application developer's responsibility to assign interrupt priorities correctly in order to achieve the desired behavior. Interrupts of the same level or lower cannot preempt each other. By setting all interrupts to the same priority (e.g., 1), interrupt nesting is effectively disabled.

### 5.1 The `qep_port.h` Header File

The QEP header file for the QK port is located in `qpc\ports\rx\qk\iar\qep_port.h`. It is identical to the non-preemptive case shown in [Listing 3](#).

### 5.2 The `qf_port.h` Header File

The QEP header file for the QK port is located in `qpc\ports\rx\qk\iar\qf_port.h`. It is almost identical to the non-preemptive case shown in [Listing 4](#), except the QF port for the QK kernel includes `tge` "`qk_port.h`" header file instead of "`vanilla.h`".

### 5.3 The `qk_port.h` Header File

As with any preemptive kernel, the QK needs to be notified about entering an interrupt context and about exiting an interrupt context in order to perform a context switch, if necessary. Additionally, in case of the RX CPU and the specific interrupt functions generated by the IAR compiler, the QK kernel must perform an **extended context switch** to preserve the state of the FPSW (Floating Point Status Word) register. The coprocessor support via the extended context switch of the QK kernel is described in Section 10.4 of [PsiCC2].

**Listing 9: ISR entry and exit in `qk_port.h`**

```
/* QK interrupt entry and exit */
(1) #define QK_ISR_ENTRY() do { \
(2)     ++QK_intNest_; \
(3)     __enable_interrupt(); \
    } while (0)

(4) #define QK_ISR_EXIT() do { \
(5)     __disable_interrupt(); \
(6)     --QK_intNest_; \
(7)     if (QK_intNest_ == (uint8_t)0) { \
```

```

(8)         uint8_t p = QK_schedPrio_(); \
(9)         if (p != (uint8_t)0) { \
(10)            _set_interrupt_level(0); \
(11)            QK_schedExt_(p); \
            } \
        } \
    } while (0)

(12) #define QK_EXT_SAVE(act_) \
(13)     ((act_)->thread = (void *)_builtin_get_fpsw())

(14) #define QK_EXT_RESTORE(act_) \
(15)     _builtin_set_fpsw((unsigned long)(act_)->thread)

#include "machine.h"          /* for _builtin_get_fpsw()/_builtin_set_fpsw() */
#include "qk.h"              /* QK platform-independent public interface */

```

- (1) The `QK_ISR_ENTRY()` macro must be invoked at the entry to the ISR code and definitely before any QP services.
- (2) With interrupts still disabled, the QK interrupt nesting level is incremented to account for entering another level of interrupt. (The QK interrupt nesting level is decremented and checked on ISR exit, discussed later.)
- (3) Interrupts are enabled via a compiler intrinsic function (remember that RX CPU enters the ISR with interrupts disabled). Note that this only sets `PSW[I] = 1` (enabled); it does not adjust the `PSW[IPL]`, the processor's interrupt priority level. Only interrupts with a priority greater than the current IPL value may preempt this ISR.
- (4) The `QK_ISR_EXIT()` macro must be the last line of a user-written ISR in C. The macro performs "exit ISR housekeeping" and transfers control to the QK scheduler if necessary.
- (5) Interrupts are disabled (`PSW[I]` set to 0) in order to safely adjust the interrupt nesting level.
- (7) The QK interrupt nesting level is decremented to account for leaving the interrupt. When the interrupt nesting value becomes 0, this indicates that the code is about to return to task level.
- (8-9) The `QK_schedPrio_()` function returns the highest priority task ready to run or zero if no task has a higher priority than the current level.
- (10) The Interrupt Priority Level in the Program Status Word register (`PSW[IPL]`) is set to 0, which corresponds to the **task level** priority. This is exactly what is described in [PSiCC2], Figure 10.2, item (6); setting IPL to zero corresponds to executing an "End of Interrupt" instruction, which means that the interrupt controller of the RX CPU stops prioritizing the current interrupt. At this point, the interrupt controller will allow any interrupt to run, which is exactly the behavior expected at task level.
- (11) The **extended** QK scheduler is invoked to keep launching the high-priority tasks as long as they are above the currently serviced priority (see [PSiCC2], Figure 10.2, items (6) through (8)). The QK scheduler is designed to be called with interrupts disabled and also returns with interrupts disabled, although it enables interrupts before launching any task.

---

**NOTE:** The **extended** QK scheduler is used, instead of the regular scheduler, to save and restore the FPSW register. The following macros `QK_EXT_SAVE()`/`QK_EXT_RESTORE()` specify how to save and restore the extended context of the FPSW.

---

- (12) The `QK_EXT_SAVE()` macro specifies the process of saving the extended context, which in the case of the RX processor is the FPSW register.
- (13) The IAR built-in function `_builtin_get_fpsw()` resolves to a single instruction "MVFC Rn".

- (14) The `QK_EXT_RESTORE()` macro specifies the process of restoring the extended context, which in the case of the RX processor is the FPSW register.
- (15) The IAR built-in function `_builtin_set_fpsw()` resolves to a single instruction “MVTc Rn”.

## 5.4 The Board Support Package for the QK Port

The BSP for the QK version is located in the file `bsp.c` in the directory `qpc/examples/rx/qk/iar/dpp-qk-yrdkrx62n\`. The BSP for QK is mostly similar to the “Vanilla” kernel discussed before. This section describes only the differences between the two kernels.

### 5.4.1 Interrupt Service Routines (ISRs) for the preemptive QK kernel

As mentioned earlier, the IAR toolset enables the user to write ISRs as interrupt functions in C/C++. These compiler-generated ISRs are perfectly adequate for the preemptive kernel, provided that the compiler generates code for saving and restoring the Accumulator in the interrupt functions. As discussed before, the IAR compiler does it only when the `--save_acc` compile-time option is defined.

---

**NOTE:** The QK port assumes and **requires** the `--save_acc` option.

---

**Listing 10: Tick timer ISR for QK in bsp.c**

```
(1) #pragma vector=28
(2) static __interrupt void tickISR(void) {
(3)     QK_ISR_ENTRY();           /* inform the QK kernel about entering the ISR */

    #ifdef Q_SPY
        l_tickTime_ += l_tickPeriod;           /* account for the clock rollover */
    #endif

    QF_TICK(&l_tickISR);           /* process all armed time events */

(4)     QK_ISR_EXIT();           /* inform the QK kernel about exiting the ISR */
}
```

- (1) The `#pragma` directs the IAR compiler to allocate the following interrupt function to the given vector.
- (2) The ISR is defined in C by means of the `__interrupt` extended keyword of the IAR compiler.
- (3) The macro `QK_ISR_ENTRY()` informs the QK kernel that the ISR has been entered. It **must** be called before invoking any QP services in the ISR body.
- (4) The macro `QK_ISR_EXIT()` informs the QK kernel that the ISR is about to be exited. It **must** be called at the very end of the ISR body.

### 5.4.2 Idle loop customization in the QK port

As described in Chapter 10 of [PSiCC2], the QK idle loop executes only when there are no events to process. The QK allows you to customize the idle loop processing by means of the callback `QK_onIdle()`, which is invoked by every pass through the QK idle loop. You can define the platform-specific callback function `QK_onIdle()` to save CPU power, or perform any other “idle” processing.

---

**NOTE:** The idle callback `QK_onIdle()` is invoked with interrupts unlocked (which is in contrast to `QF_onIdle()` that is invoked with interrupts locked, see Section 6).

---

**Listing 11: Idle callback QK\_onIdle() for the QK kernel in bsp.c**

```
(1) void QK::onIdle(void) {  
  
    (2)     QF_INT_DISABLE();  
    (3)     BSP_LED_IDLE_ON();           // toggle the User LED on and then off, see NOTE02  
    (4)     BSP_LED_IDLE_OFF();  
    (5)     QF_INT_ENABLE();  
  
    (6) #ifdef Q_SPY  
        . . .  
    (7) #elif defined NDEBUG  
    (8)     __wait_for_interrupt();  
        #endif  
    }
```

- (1) The idle callback for the QK kernel is always entered with interrupts enabled.
- (2) Interrupts are disabled to toggle the idle LED.
- (3-4) The idle LED (LED12 of the YRDKRX62N board) is toggled on and off each time through the idle callback. Thus, a brighter LED indicates more idle time. A heavily loaded CPU will spend little or no time in the idle loop and thus the idle LED would be dim. Note that in a release build, the CPU will sleep most of the time, and the LED will be toggled only at the rate of the interrupts that wake up the CPU. In a debug build variant, the CPU never sleeps, and the LED's intensity gives a good indication of the idle task activity.
- (5) Interrupts are re-enabled after toggling the idle LED.
- (6) The software-tracing code is conditionally compiled into the build when enabled at compile time. When using QS, the trace data is sent out during idle loop processing. If the UART's Transmit Data Register (TDR) is empty, this code calls a QSPY API to see if there is another byte of data to send out the serial port.
- (7) In release mode (no debugger) the CPU can be put to low-power sleep.
- (8) The `__wait_for_interrupt()` intrinsic provided by the IAR compiler simply inserts a `WAIT` instruction to the RX CPU. (More advanced power management could be performed here; this port only sleeps the CPU, and does not put any other peripheral in low-power mode).

## 6 QS Software Tracing Instrumentation

Quantum Spy (QS) is a software tracing facility built into all QP components and also available to your application code. QS allows you to gain unprecedented visibility into your application by selectively logging almost all interesting events occurring within state machines, the framework, the kernel, and your application code. QS software tracing is minimally intrusive, offers precise time-stamping, sophisticated runtime filtering of events, and good data compression (please refer to “QSP Reference Manual” section in the “QP/C Reference Manual” and also to Chapter 11 in [PSiCC2]).

This QDK demonstrates how to use the QS to generate real-time trace of a running QP application. Normally, the QS instrumentation is inactive and does not add any overhead to your application, but you can turn the instrumentation on by defining the Q\_SPY macro and recompiling the code. In this QDK, this means selecting and building the "Spy" variant of the code (as opposed to the Debug or Release variant).

QS can be configured to send the real-time data out of the serial port of the target device. On the YRDKRX62N evaluation board, QS uses SCI2 in asynchronous (UART) mode to send the trace data out of DB9 connector J5 "COMM PORT". The YRDKRX62N kit does not come with a serial cable, you will need to provide this. In all likelihood, you will need to use a serial-to-USB cable/adaptor as nowadays it is difficult to find a computer with a standard DB9 serial port.

---

**NOTE:** This port uses the serial port (configured for 115,200 baud by default) as the output port for sending QSPY trace data.

---

### 6.1 QS initialization in QS\_onStartup()

The routine `QS_onStartup()` is invoked during initialization to initialize and configure the QSPY tracing buffer, timing variables, and trace data transmit UART.

**Listing 12: QS initialization in bsp.c**

```
(1) uint8_t QS_onStartup(void const *arg) {
(2)     static uint8_t qsBuf[6*256];           /* buffer for Quantum Spy */
(3)     QS_initBuf(qsBuf, sizeof(qsBuf));

                                     /* Configure & enable the serial interface used by QS */
(4)     . . .

     /* Initialize QS timing variables */
(5)     QS_tickPeriod_ = TICK_COUNT_VAL;
(6)     QS_tickTime_   = 0;                 /* count up timer starts at zero */
(7)     QS_FILTER_ON(QS_ALL_RECORDS);
(8)     QS_FILTER_OFF(QS_QF_ACTIVE_ADD);
     . . .
     QS_FILTER_OFF(QS_QF_ISR_EXIT);

(9)     return (uint8_t)1;                 /* return success */
}
```

- (1) The `QS_onStartup()` routine is called when the BSP is initialized through the macro `QS_INIT()`.
- (2) Trace data to be sent out the serial port is enqueued in this buffer. Adjust the size of this buffer based on your application's tracing needs. The bursts of volume of data being traced / transmitted, and the serial baud rate will impact the size required.
- (3) `QS_initBuf()` is called to initialize the output buffer.

- (4) This omitted piece of code performs the hardware-specific initialization of the UART used by QSPY. QSPY uses the YRDKRX62N's single serial comm port, which is connected to Serial Communications Interface #2 (SCI2) on the RX62N. Chip-specific details of the UART initialization are not shown here, but they are heavily commented in the source code and reference sections in the chip's manual.
- (5-6) `QS_tickPeriod_` is initialized and never changes. This is the value that timer peripheral CMT0 (used for the OS tick timer) counts up to before matching & resetting to zero before counting up again. `QS_tickTime_` increments by an amount of `QS_tickPeriod_` each time a kernel tick timer interrupt is handled. The description of `QS_onGetTime()` later describes use of these values.
- (8) Here we enable all QS trace records, and then selectively disable some of them. Deciding which data to trace is a subject covered in depth in Chapter 11 of [PSiCC2] and is not specific to this port.
- (9) We return 1 to indicate initialization was successful.

## 6.2 QS Trace Output in `QF_onIdle()/QK_onIdle()`

To be minimally intrusive, the actual output of the QS trace data happens when the system has nothing else to do, that is, during the idle processing. The following listing shows the code placed either in the `QF_onIdle()` callback ("Vanilla" port), or `QK_onIdle()` callback (in the QK port):

**Listing 13: QS trace output in `bsp.c`**

```

void QF_onIdle(void) {
    . . .
(1) #ifdef Q_SPY
        /* RX62N has no TX FIFO, just a Transmit Data Register (TDR) */
(2)     if (SMCI2.SSR.BIT.TDRE) { /* Is SMC's TDR Empty? */
(3)         uint16_t b;

(4)         QF_INT_DISABLE();
(5)         b = QS_getByte();
(6)         QF_INT_ENABLE();

(7)         if (b != QS_EOD) {
            SMCI2.TDR = (uint8_t)b; /* send byte to UART TDR */
        }
    }
    . . .

```

- (1) The code is only compiled into the `Q_SPY` build configuration.
- (2) The UART's TDRE status flag is checked to see if the Transmit Data Register is Empty.
- (3) Interrupts are disabled to protect the QS output trace buffer while it is being accessed from non-interrupt code. Otherwise, this idle loop processing could be interrupted by an ISR which could try to access the trace buffer and corrupt it (shared resource problem).
- (4) The temporary variable for storing the return from the `QS_getByte()` API call must be 16-bit wide.
- (4) The `QS_getByte()` returns the next byte of trace data or `QS_EOD` if no data is available.
- (5) Once access to the trace buffer is complete, interrupts can safely be re-enabled.
- (6) If the returned data is not `QS_EOD` (end of data), the data needs to be sent out
- (7) A byte of trace data is written into the Transmit Data Register and sent out the UART.

### 6.3 QS Time Stamp Callback QS\_onGetTime()

The platform-specific QS port must provide function `QS_onGetTime()` (Listing 9(12)) that returns the current time stamp in 32-bit resolution. To provide such a fine-granularity time stamp, the RX port uses the CMT0 facility, which is the same timer already used for generation of the system clock-tick interrupt.

---

**NOTE:** The `QS_onGetTime()` callback is always called with interrupts disabled.

---

**Listing 14: QS initialization in bsp.c**

```
(1) QSTimeCtr QS_onGetTime(void) { /* invoked with interrupts locked */
(2)     if (IR(CMT0, CMI0)) { /* is tick ISR pending? */
(3)         return l_tickTime_ + CMT0.CMCNT + l_tickPeriod_ ;
        }
        else { /* no rollover occurred */
(4)         return l_tickTime_ + CMT0.CMCNT;
        }
    }
```

- (1) `QS_onGetTime()` is a very important function. It provides a high-resolution time-stamp for outgoing trace records. It is invoked at the time a trace record is appended to the trace record by the application (as opposed to when the record is transmitted). This routine is called with interrupts disabled.
- (3) We check to see if the tick timer interrupt on timer peripheral CMT0 is already pending. (it could be pending, because interrupts are disabled inside the `QS_onGetTime()` callback).
- (4) If timer peripheral CMT0 has a pending interrupt, this indicates that the free-running counter CMCNT has already counted up to its target match value and has been re-loaded with 0 again. Thus, in order to get an accurate timestamp, the overflow must be accounted for by adding an extra number of ticks (stored in `QS_tickPeriod_`) in addition to the step described in item

---

**NOTE:** The CMT0 interrupt (the system clock tick) could be pending at this time, because interrupts are disabled. Once interrupts are re-enabled, the timer interrupt will fire, `QS_timeTick_` will be incremented by `QS_tickPeriod_` in the tick ISR as we have seen, and the timer interrupt pending flag will be cleared.)

---

- (5) If the timer interrupt is not pending, the current timestamp is the sum of the long-term value in `QS_timeTick_`, which is updated in fairly large increments, and the instantaneous value in the free running timer counter register CMCNT in peripheral CMT0. The counter is an up-counter, so this is a simple addition.

### 6.4 Running the QSpy host application

The QSPY host application receives the QS trace data from the target, parses it and displays on the host workstation (currently Windows, Linux, or Mac OS X). For the configuration options chosen in this port, you invoke the QSPY host application as follows (please refer to “QSP Reference Manual” section in the “QP/C Reference Manual” and also to Chapter 11 in [PsiCC2]):

```
qspy -cCOMx
```

---

**NOTE:** COMx will be something like COM1, COM2, etc. depending on your machine's serial port availability and configuration.

---

## 7 Related Documents and References

Document	Location
[PSiCC2] “Practical UML Statecharts in C/C++, Second Edition”, Miro Samek, Newnes, 2008	Available from most online book retailers, such as <a href="http://www.amazon.com">Amazon.com</a> . See also: <a href="http://www.state-machine.com/psicc2.htm">http://www.state-machine.com/psicc2.htm</a>
[QP/C 08] “QP/C Reference Manual”, Quantum Leaps, LLC, 2010	<a href="http://www.state-machine.com/doxygen/qpc/">http://www.state-machine.com/doxygen/qpc/</a>
[QP/C++ 08] “QP/C++ Reference Manual”, Quantum Leaps, LLC, 2010	<a href="http://www.state-machine.com/doxygen/qpcpp/">http://www.state-machine.com/doxygen/qpcpp/</a>
[QL AN-Directory 07] “Application Note: QP Directory Structure”, Quantum Leaps, LLC, 2007	<a href="http://www.state-machine.com/doc/AN_QP_Directory_Structure.pdf">http://www.state-machine.com/doc/AN_QP_Directory_Structure.pdf</a>
[QL AN-DPP 08] “Application Note: Dining Philosopher Problem Application”, Quantum Leaps, LLC, 2008	<a href="http://www.state-machine.com/doc/AN_DPP.pdf">http://www.state-machine.com/doc/AN_DPP.pdf</a>
IAR C/C++ Compiler Reference Guide for the Renesas RX Microcomputer Family	<a href="http://supp.iar.com/FilesPublic/UPDINFO/004631/EWR_X_CompilerReference.ENU.pdf">http://supp.iar.com/FilesPublic/UPDINFO/004631/EWR_X_CompilerReference.ENU.pdf</a>
Renesas Demonstration Kit (YRDKRX62N) for RX62N User’s Manual: Hardware [REU10B0009-0100]	Available from the YRDKRX62N kit CD-ROM & downloaded from Renesas website as well
RX621 Group: Datasheet [REJ03B0281-0050]	Available from the YRDKRX62N kit CD-ROM & downloaded from Renesas website as well
RX62N Group, RX621 Group: User’s Manual: Hardware [R01UH0033EJ0111]	Available from the YRDKRX62N kit CD-ROM & downloaded from Renesas website as well
RX62N Group, RX621 Group: User’s Manual: Software [REJ09B0435-0100]	Available from the YRDKRX62N kit CD-ROM & downloaded from Renesas website as well

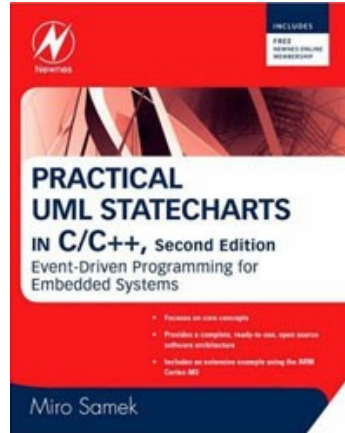
## 8 Contact Information

**Quantum Leaps, LLC**  
103 Cobble Ridge Drive  
Chapel Hill, NC 27516  
USA

+1 866 450 LEAP (toll free, USA only)  
+1 919 869-2998 (FAX)

e-mail: [info@quantum-leaps.com](mailto:info@quantum-leaps.com)

WEB : <http://www.quantum-leaps.com>  
<http://www.state-machine.com>



*“Practical UML Statecharts in C/C++, Second Edition: Event-Driven Programming for Embedded Systems”, by Miro Samek, Newnes, 2008*

